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08/965,286	11/06/1997	TAKAYUKI GOMI	P97.2608	3718

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 08/965,286	Applicant(s) GOMI ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003* .

2a)☒ This action is **FINAL**. .2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6,20-26 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,20-26 and 30-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Kumamaru et al. (4,379,726).

Kumamaru et al. teach in figure 10 a semiconductor device having a first vertical bipolar transistor 15 and a second vertical type transistor 13 having a breakdown voltage that is higher than that of the first vertical type transistor, formed on a P type semiconductor substrate comprising a first conductivity type silicon substrate 1, 5, an epitaxial layer 11 formed on the substrate above the datum surface, a first embedded diffusion layer 14 formed as part of a first vertical bipolar transistor 15 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 13 (see figure 8) formed as part of a second vertical type transistor 13 directly on the substrate,

wherein the second embedded diffusion layer 13 having an impurity concentration that is less than an impurity concentration of the first embedded diffusion layer 14, and

wherein a top and a bottom of the second embedded diffusion layer 13 are formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between the top and bottom of the first embedded diffusion layer 14 and a surface of the emitter of the first vertical type bipolar transistor, respectively.

Claim Rejections - 35 USC ' 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 6, 20-26 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. (4,379,726) in view Yamauchi (5,151,765) or Takemoto et al.

Kumamaru et al. teach in figure 10 a semiconductor device having a first vertical bipolar transistor 15 and a second vertical type transistor 13 having a breakdown voltage that is higher than that of the first vertical type transistor, formed on a P type semiconductor substrate comprising a first conductivity type silicon substrate 1, 5, an epitaxial layer 11 formed on the substrate above the datum surface, a first embedded diffusion layer 14 formed as part of a first vertical bipolar transistor 15 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity

concentration than that of the epitaxial layer, a second embedded diffusion layer 13 (see figure 8) formed as part of a second vertical type transistor 13 directly on the substrate, wherein a top and a bottom of the second embedded diffusion layer 13 are formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between the top and bottom of the first embedded diffusion layer 14 and a surface of the emitter of the first vertical type bipolar transistor, respectively.

Kumamaru et al. do not a state that the first and second embedded diffusion layers are formed as a part of the respective collector regions.

Yamauchi teaches in figure 5 first and second embedded diffusion layers 2a, 2b are formed as a part of the respective collector regions 3a, 3b, and connected to collector contact regions 7a, 7b.

Takemoto et al. teach in figure 5 first and second embedded diffusion layers 32, 36 are formed as a part of the respective collector regions 33 and 39, respectively (column 6, lines 34-41).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to characterize the first and second embedded diffusion layers as being a part of the respective collector regions in Kumamaru et al.'s device because the embedded diffusion layers the collector regions, the epitaxial layer and the collector contact regions are all effectively become part of a collector layer due to their identical conductivity type.

Regarding claims 4 and 21, although figure 10 of Kumamaru et al. does not depict a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer, at all distances greater than a distance from the surface of the emitter of the second vertical type bipolar transistor to a peak position of the impurity concentration of the second embedded diffusion layer, this feature is inherent in Kumamaru et al.'s device, because it is well known in the art that diffused areas have concentration that follows natural distribution curve, of which official notice is taken (See Watanabe et al., figure 9, graph 22"). In the alternative, the second embedded diffusion layer can comprise layers 13 and 12. Thus, the second embedded diffusion layer has impurity concentration portions that are equal and greater than that of the epitaxial layer, as claimed.

Regarding claim 6, Kumamaru et al. do not teach a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Kumamaru et al.'s device, since it is within the skills of an artisan to form a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15, subject to routine experimentation and optimization, respectively. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are

disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 22, Kumamaru et al. teach a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the surface of the emitter that is approximately equal to a location of the bottom of the first embedded diffusion layer from the surface of the emitter.

Regarding claim 23, Kumamaru et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type bipolar transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Regarding claims 20 and 24, Kumamaru et al. teach substantially the entire claimed structure, as applied to claim 1 above, including first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers to define first and second epitaxial thicknesses, respectively, wherein

the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

Regarding claim 26, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

Regarding claims 30 and 31, the first vertical type bipolar transistor is capable of operating at a higher speed and a lower voltage tan the second vertical type bipolar transistor.

Response to Arguments

Applicant argues that Kumamaru et al. do not teach a top and a bottom of the second embedded diffusion layer are formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between the top and bottom of the first embedded diffusion layer and a surface of the emitter of the first vertical type bipolar transistor, respectively.

Figure 10 of Kumamaru et al. clearly depicts a top and a bottom of the second embedded diffusion layer 13 being formed at a distance from a surface of the emitter of the second vertical type bipolar transistor greater than a distance between the top and bottom of the first embedded diffusion layer 14 and a surface of the emitter of the first vertical type bipolar transistor, respectively, as claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 8, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800